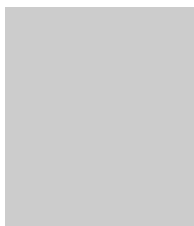





PERSONAL INFORMATION

Amăricăi-Boncalo Oana



 Bulevardul Vasile Pârvan, Nr. 2, Room B522, Timișoara, 300223, România
 0256403264
 oana.boncalo@cs.upt.ro

Gender Female | Birth-date 14/07/1983 | Nationality Romania

PROFESIONAL EXPERIENCE

Feb 2009 – Sept 2012

Assistant Professor

Computing Engineering Department
 Universitatea Politehnica Timișoara

Oct 2012 – present

Lecturer

Computing Engineering Department
 Universitatea Politehnica Timișoara

Education

Dec 2008

PhD

Universitatea Politehnica Timișoara
 Phd Thesis: Simulation Based Assessment of Quantum Circuit Reliability

June 2006

Bachelor in Engineering

Universitatea Politehnica Timișoara

LANGUAGE COMPETENCES

Maternal Languages

Romanian

Foreign Languages

	UNDERSTANDING		SPEECH		SCRIRE
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1

Diving License

▪ Yes

ADDITIONAL INFORMATION

Relevant Journal Publications

1. O. Boncalo, A. Amaricai, V. Savin, D. Declercq, F. Ghaffari - Check node unit for LDPC decoders based on one-hot data representation of messages - IET Electronics Letters, Vol. 51, No. 12, pp. 907-908, 2015
2. A. Amaricai, O. Boncalo, C.E. Gavriliu - Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays – IET Computing and Digital Techniques, Vol.8, Issue 4, pp. 187-197, 2014
3. A. Amaricai, O. Boncalo – FPGA Implementation of Very High Radix Division with Prescaling – IET Electronic Letters, September 2012
4. A. Amaricai, M. Vladutiu, O. Boncalo - Design Issues and Implementations for Floating-Point Divide-Add Fused – IEEE Transactions on Circuits and Systems II (Express Briefs), Vol. 57, Issue 4, April, 2010
5. O. Boncalo, A. Amaricai, M. Udrescu, M. Vladutiu - Quantum circuit's reliability assessment with VHDL-based simulated fault injection - Microelectronics Reliability, Volume 50, Issue 2, February 2010

Relevant Conference Publications

1. O. Boncalo, P.F. Mihancea, A. Amaricai - Template-Based QC-LDPC Decoder Architecture Generation – Proc. Int. Conf. on Information Communication and Signal Processing, ICICS, 2015 (Accepted)
2. O. Boncalo, A. Amaricai, V. Savin - Memory efficient implementation of self-corrected min-sum LDPC decoder – Proc. IEEE Int. Conf. on Electronic Circuits and Systems (ICECS), 2014
3. O. Boncalo, A. Amaricai, C. Spagnol, E. Popovici - Cost effective FPGA probabilistic fault emulation - Proc. NORCHIP, 2014
4. O. Boncalo, A. Amaricai, A. Hera, V. Savin - Cost-efficient FPGA layered LDPC decoder with serial AP-LLR processing - Proc. FPL, 2014
5. O. Boncalo, A. Dobre, A. Amaricai, A. Tanase - Using Cycle-Approximate Simulation for Bus Based Multi-Processor System-On Chip Analysis – Proc. 5th International ICST Conference on Simulation Tools and Techniques (SIMUTOOLS), 2012

Main Research Projects

1. UEFISCDI-ANR Bilateral Project DIAMOND – Universitatea Politehnica Timisoara (UPT), CEA-LETI, ETIS-ENSEA – UPT Principal Investigator
2. CHIST-ERA GEMSCLAIM – Univ. Innsbruck, Queens Univ. of Belfast, RWTH Aachen, UPT – 2012-2015, Researcher
3. POSCCE-499-11844 “FALX DACIAE” – Movidius, UPT – 2010-2012, Researcher